



PATENTS
15311-2107

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re The Application of:)
Gilbert M. Wolrich et al.)
Serial No.: 09/042,417)
Filed: March 13, 1998)
For: Reduction of Add-Pipe Logic by Op-)
erand Offset Shift)
)

Examiner: Firmin Backer

Art Unit: 2155

Cesari and McKenna, LLP
88 Black Falcon Avenue
Boston, MA 02210
January 19, 2001

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X Request for Reconsideration

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Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

REQUEST FOR RECONSIDERATION

Applicants respectfully request that the Examiner reconsider the rejections set forth in his Office action dated October 20, 2000.

The invention to which the above-identified patent application's claims are directed concerns the "add pipe" in a floating-point processor. Signals (OPERAND_A and OPERAND_B) representing two floating-point operands and consisting of respective sign signals (SIGN_A and SIGN_B), mantissa signals (FRAC_A and FRAC_B), and exponent signals (EXP_A and EXP_B) are introduced at the top of Fig. 5, and circuitry de-

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picted in Fig. 5 and Fig. 4 produce an output signal consisting of sign (SIGN), mantissa (FRAC), and exponent (EXP) signals.

Among the functions performed by the Fig. 5 circuitry is to determine which of the operands is greater in magnitude and to produce, as indicated at the top of Fig. 4, mantissa signals (RAW_FRAC_MIN) and (RAW_FRAC_SUB) respectively representing the larger and smaller operands' mantissas. Shift circuitry 30 and 32 performs normalization and/or alignment shifting on these operands and applies the results to a main mantissa addition/subtraction circuit 34, which Fig. 12 depicts in more detail.

As Fig. 12 shows, mantissa addition/subtraction circuitry can be quite complex. And the discussion set forth in the passage beginning at page 16's line 16 and continuing through page 18's line 14 describes further complexity that this mantissa addition/subtraction circuitry would conventionally require for rounding purposes. As the passage beginning in page 24's line 10 explains, though, floating-point circuitry that employs the invention's teachings can avoid this additional complexity.

Specifically, the inventors recognized that this circuitry would not need to be as complex—and that it could therefore be made significantly faster—if, as the specification passage beginning at page 6's line 14 and extending through page 7's line 15 describes in detail, the mantissa shifting that Fig. 4's shifters 30 and 32 perform on the mantissas applied to the mantissa addition/subtraction circuitry 34 were, for some pairs of numbers, different when the operation to be performed is effective addition from what it is when the operation is effective subtraction. The claims define this concept: claim 1 specifies that mantissa-processing circuitry so applies respective processed mantissa signals to the

main mantissa adder “that, for at least some pairs of mantissas, the mantissa signals applied to the main mantissa adder when the main mantissa adder is to subtract a pair of mantissas are offset to the left by one position from the mantissa signals applied thereto when the main mantissa adder is to add the same pair of mantissas.”

The Examiner has rejected both this claim and all of the remaining claims, which depend on it, under 35 U.S.C §§112 and 103. Applicants respectfully request that the Examiner reconsider both grounds of rejection.

The Examiner bases his rejection under the second paragraph of §112 on “the limitation ‘the mantissas’ in paragraph 3 lines 15-18.” Specifically, the Examiner says, “This limitation is vague and does not offer a clear understanding of what is being claimed.” But that statement is merely conclusory. The Examiner does not state why he considers the limitation vague and how one could fail to obtain a clear understanding of what it defines. Moreover, a perusal of claim 1 reveals no recitation of “the mantissas” in claim 1’s lines 15-18. So Applicants respectfully request that the Examiner state a clearer basis for this ground of rejection if he intends to persist in it.

Applicants also respectfully request that the Examiner reconsider his rejection of all claims under 35 U.S.C §102(b) as being anticipated by U.S. Patent No. 5,276,634 to Suzuki et al. since, contrary to the Examiner’s contention, nothing in the Suzuki et al. patent discloses or suggests the differential-mantissa-shift feature defined by claim 1’s recitation that “the mantissa signals applied to the main mantissa adder when the main mantissa adder is to subtract a pair of mantissas are offset to the left by one position from

the mantissa signals applied thereto when a main mantissa adder is to add the same pair of mantissas."

Applicants have carefully reviewed the Suzuki et al. patent and especially the passages to which the Examiner invited particular attention. While various of them deal with mantissa addition and subtraction and with shifting for various purposes, none teaches the differential pre-shift mentioned above, explained in Applicants' specification, and defined by the claims.

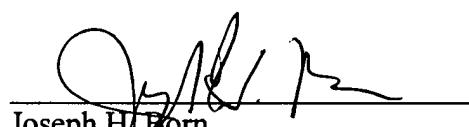
It is apparently the following portion of the Examiner's eighth paragraph that is directed particularly to the differential pre-shift: "Suzuki et al. teach . . . subtracting a pair of mantissas when they are offset to the left by one position from the applied mantissa signals and add when the pair of mantissas are the same (see Fig. 1, 2, 14, column 1 line 18-29, column 11 lines 12—18) (see also claims 1, 10, 17)." But this statement of the Examiner's is unclear because it seems to say that mantissas are offset from applied mantissa signals, i.e., that somehow the mantissas are offset from the signals that represent them. It also seems to say that a decision as to whether to add or subtract is made in accordance with whether this (unintelligible) condition prevails. At most, though, that would be the reverse of Applicants' differential pre-shift. Applicants' differential pre-shift is not an addition-or-subtraction decision but rather a shifting of the signals based on whether the operation to be performed is addition or subtraction. More important, the particular Suzuki et al. excerpts to which the Examiner particularly refers do not at all support the statements that he bases on them. Lines 18-29 of Suzuki et al.'s column 1, for instance, merely set forth a general description of mantissa addition and subtraction,

apparently indicating that the operation to be performed depends on the operands' signs. The other specification passage, namely, lines 12-18 of Suzuki et al.'s column 11, merely deal with exponent offset employed in exponent subtraction used for floating-point division: it does not deal with mantissa addition or subtraction at all. And the particular Suzuki et al. claims on which the Examiner relies add nothing.

In short, Suzuki et al. neither disclose nor suggest the invention that claim 1 defines and therefore neither disclose nor suggest any dependent claim's subject matter. Applicants therefore respectfully request that the Examiner reconsider and withdraw all claim rejections and allow the application as previously amended.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,



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